

METHOD OF ENLARGING CONTACT AREA OF A GATE ELECTRODE, SEMICONDUCTOR
DEVICE HAVING A SURFACE-ENLARGED GATE ELECTRODE, AND METHOD OF
MANUFACTURING THE SAME

Application No. NEW - Attorney Docket No. SEC.1134

Inventor(s): Chan-Hyung CHO et al.

FIG. 1A

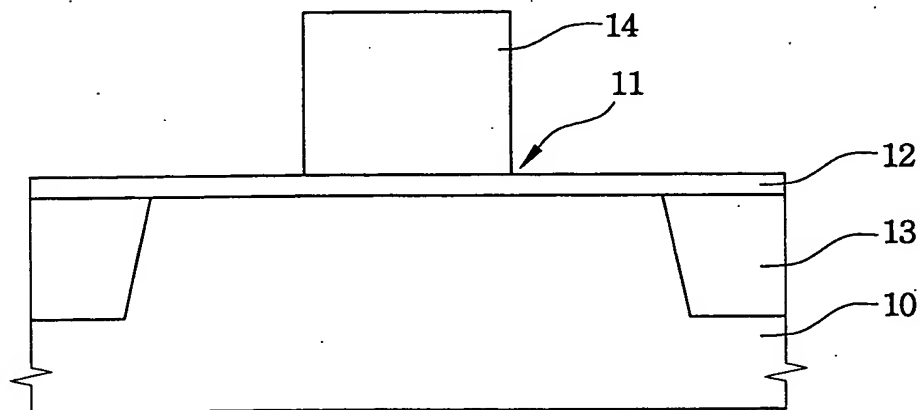
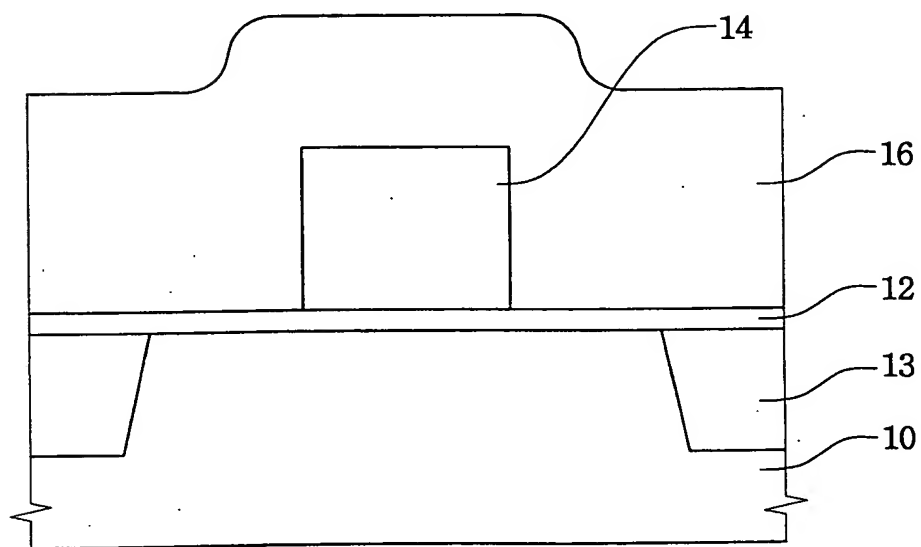


FIG. 1B



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FIG. 1C

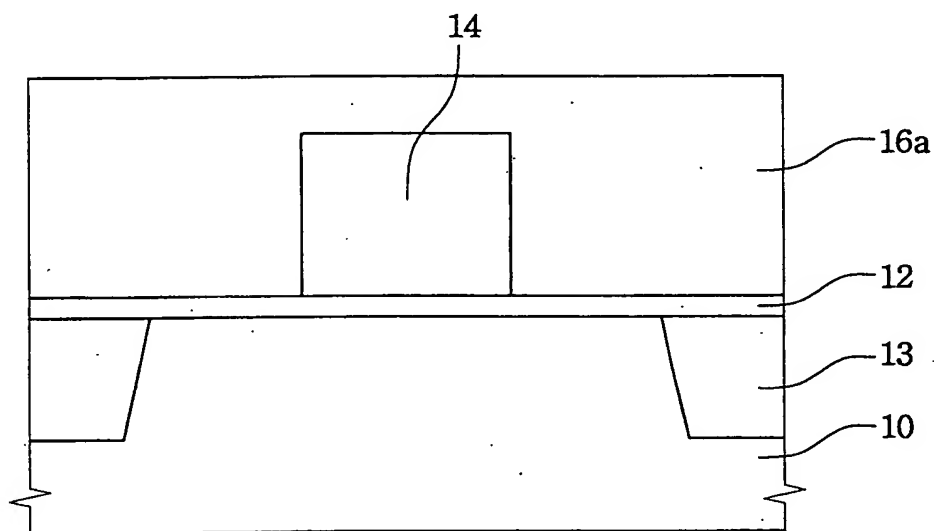
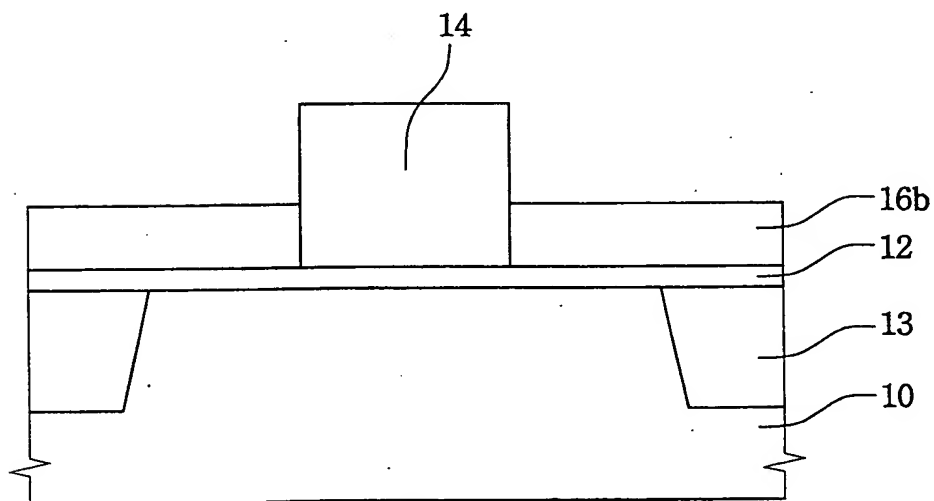


FIG. 1D



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Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 10 with a trench 13. A gate stack 12 is formed on the substrate 10, and a gate 14 is formed on the gate stack 12. A gate spacer 16b is formed on the side of the gate stack 12. A gate electrode 18 is formed on top of the gate stack 12.

Fig. 1 is a cross-sectional view of a semiconductor device. A substrate 10 is shown with a trench 13. A gate 12 is formed on the substrate 10, and a gate oxide 16b is formed on the gate 12. A gate electrode 14 is formed on the gate oxide 16b, and a gate insulating layer 19 is formed on the gate electrode 14.

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FIG. 1G

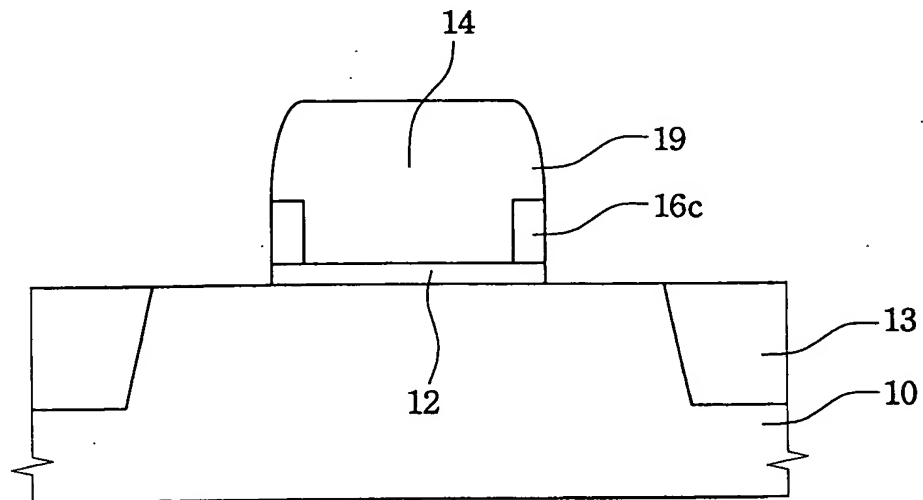
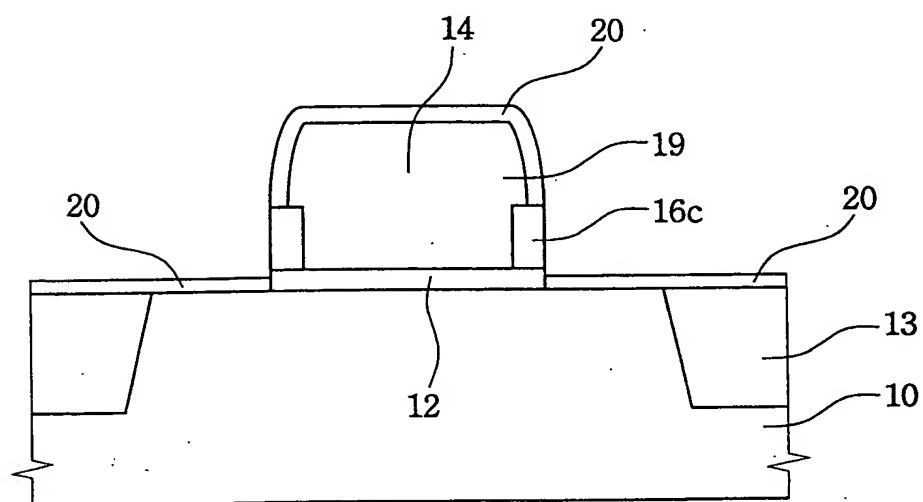


FIG. 1H



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This cross-sectional view shows a central dome-shaped structure (14) with a top surface (19) and side surface (20). The dome is supported by a base layer (12) which has two rectangular protrusions (22a, 22b) on its top surface. The base layer is situated on a substrate (10) which has a recessed region (13) on its top surface. A layer (16c) is located between the base layer (12) and the substrate (10). Arrows indicate the direction of light or signal passing through the structure.

This cross-sectional view shows a central cavity 14 defined by a top layer 16c and side walls 19. The cavity is situated within a substrate 10 that has a top layer 12 and a bottom layer 13. The substrate is supported by a base 20. The side walls 19 are connected to the top layer 16c by vertical structures 22a and 22b. A layer 23 is shown on the top surface of the substrate 10, and a layer 20 is shown on the bottom surface of the substrate 10.

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A cross-sectional view of a semiconductor device. A central layer 14 is positioned on a substrate 10. The central layer 14 is flanked by two side layers 24. The side layers 24 are connected to a common layer 12. The common layer 12 is further connected to a layer 16c. The entire structure is surrounded by a layer 20. The substrate 10 is shown with a cross-section line 13.

This cross-sectional view shows a semiconductor device with a central gate structure. The device includes a substrate 10 with a layer 12 on top. A central gate structure 14 is formed on layer 12, with a gate dielectric 19 and a gate electrode 20. The gate structure is flanked by side regions 22a and 22b, which are separated by a central channel 26. The side regions are covered by a layer 24, which is part of a larger layer 20. The device is shown with a cross-section of a trench 13 on the right side, and a cross-section of a trench 16c on the left side. Arrows indicate the direction of light or electron beam incidence.

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